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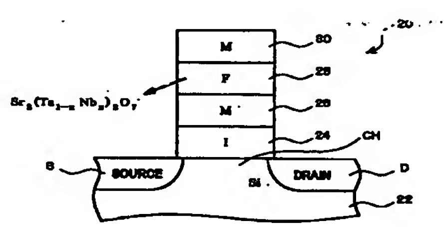
(54) FERROELECTRIC MEMORY ELEMENT AND METHOD OF PRODUCING THE SAME

(57) A ferroelectric layer having a low dielectric constant which is used for a ferroelectric memory element is provided. Also, the ferroelectric layer having a high melting point used for the ferroelectric memory element is provided. An FET 20 has a stacked structure including a gate oxidation layer 24, a floating gate 26, a ferroelectric layer 28, and a control gate 30 deposited on a channel region CH in that order, the channel region CH being formed in a semiconductor substrate 22 made of silicon. The ferroelectric layer 28 is consist of a thin film made of a mixed crystal composed of $Sr_2(Ta_{1-x}Nb_x)_2O_7$. The crystal structure of both $Sr_2Nb_2O_7$ and $Sr_2Ta_2O_7$ is pyramid quadratic structure, and their lattice constants are similar to each other. Their relative dielectric constants are in low, and their melting points are at high. Curie temperature related with their ferroelectricity is, however, too high in $Sr_2Nb_2O_7$ and too low in $Sr_2Ta_2O_7$. In order to overcome the discrepancies, the ferroelectric layer 28 having desired curie temperature is formed with a mixed crystal made of $Sr_2(Ta_{1-x}Nb_x)_2O_7$.

FIG.1



20:FET
22:SILICON SEMICONDUCTOR SUBSTRATE
24:GATE OXIDATION LAYER
26:FLOATING GATE
28:FERROELECTRIC LAYER
30:CONTROL GATE
CH:CHANNEL REGION

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Description

Cross-Reference to Related Application

[0001] The entire disclosure of Japanese Patent Application No. Hei 9-133965 filed on May 23, 1997 including specification, claims drawings and summary is incorporated herein by reference in its entirety.

Field of the Invention

[0002] The present invention relates to a ferroelectric memory device, more specifically, to ferroelectric materials used for a ferroelectric memory device.

Background art

[0003] Field effect transistors (FETs) using a ferroelectric layer is proposed as a nonvolatile memory device. An example of an FET using a PZT ($PBZr_x Ti_{1-x}O_3$) is shown in Fig. 13. The FET 12 shown in Fig. 13 is a kind of FET having a structure so called MFMIS (Metal Ferroelectric Metal Insulator Silicon). The FET 12 is formed by means of disposing a gate oxidation layer 4, a floating gate 6, a ferroelectric layer 8, and a control gate 10 in that order on a channel region CH formed in a semiconductor substrate 2.

[0004] The polarization of the ferroelectric layer 8 is turned over when a positive voltage +V is applied to the control gate 10 while grounding the substrate 2 of the FET 12 (an N channel substrate). Negative electric charges are established in the channel region CH as a result of a remanence polarization remained in the ferroelectric layer 8 even when the positive voltage +V no long be applied to the control gate 10. A condition that the negative electric charges are in the channel region CH corresponds to data "1".

[0005] On the contrary, occurrence of another polarization reversal in the opposite polarity is observed when a negative voltage -V is applied to the control gate 10. Positive electric charges are generated in the channel region CH as a result of a remanence polarization remained in the ferroelectric layer 8 even when the negative voltage -V no long be applied to the control gate 10. Another condition that the positive electric charges are in the channel region CH corresponds to data "0". Either of data "1" or data "0" is stored in the FET 12 by carrying out the procedures described above.

[0006] In order to read out the data being stored therein, a readout voltage Vr is applied to the control gate 10. The readout voltage Vr is set at a value between the threshold voltage Vth1 of the FET 12 which is defined when the data "1" is stored and the threshold voltage Vth0 of the FET 12 which is defined when the data "0" is stored. Judgement of the stored data, either in "1" or "0" can be carried out by detecting whether a drain current predetermined flows or not when the readout voltage Vr is applied to the control gate 10. The stored data never be erased after read out the data.

[0007] Thus, nondestructive readout can be carried out using the FET including a ferroelectric layer. Further, such device is capable of composing one memory cell.

[0008] However, the FET using the ferroelectric described above has the following problems to be resolved. The FET 12 is considered in a condition that a capacitor Cf (capacity Cf) which includes the ferroelectric layer 8 and a capacitor Cox (capacity Cox) having the gate oxidation layer 4 is connected in series during the writing (see Fig. 2). Under the circumstances, a divided voltage Vf defined by the following equation is applied to the capacitor Cf when a voltage (equal to either of +V or -V) is applied at a point located between the substrate 2 and the control gate 10,

$$Vf=Cox/(Cf+Cox) \cdot V.$$

[0009] On the other hand, in order to cause the polarization reversal of the ferroelectric layer 8 during the writing, the divided voltage Vf need to be a large value. And, the capacitance of the capacitor Cf should be a small value relative to that of the capacitor Cox as it is clear from the equation shown in above. The relative dielectric constant (200 to 1,000) of the PZT composing the ferroelectric layer 8 is much higher than the relative dielectric constant (3.9) of the Sio_2 which composes the gate oxidation layer 4.

[0010] Consequently, it is difficult to increase the divided voltage Vf shown in above. It is therefore, not easy to cause polarization reversal of the ferroelectric layer 8 during the writing. The melting point of PZT is at a low temperature (800 to 900°C) because PZT contains Pb. This leads lattice defects in an FET requiring heat treatment after forming a ferroelectric layer. Similar problem to PZT may be observed in a ferroelectric material using bismuth (Bi).

Disclosure of the present invention

[0011] It is an object of the present invention to overcome the above mentioned drawbacks associated with prior arts, and to provide a ferroelectric layer having a low dielectric constant which is used for a ferroelectric memory element. It is another object of the present invention to provide a ferroelectric layer having a high melting point which is used for a ferroelectric memory element.

[0012] In accordance with characteristics of the present invention, there is provided a ferroelectric memory device includes a ferroelectric layer in which information being stored using its hysteresis characteristics, wherein the ferroelectric layer is composed of a mixed crystal defined by expressions of;

$$(A1_{y1}A2_{y2}\cdots An_{yn})_2(B1_{x1}B2_{x2}\cdots Bm_{xm})_2O_7,$$
and wherein $x1+x2+\cdots+xm=1$,
and wherein $y1+y2+\cdots+yn=1$,

and wherein each of x1,x2,⋯xm, y1,y2,⋯yn has a value equal to or greater than 0, and equal to or less than 1,

and wherein at least two of x1,x2,⋯xm, y1,y2,⋯yn have values greater than 0, and less than 1,

and wherein each of A1, A2,⋯, An is an element selected so as to be different from one another from a group consisting of elements belong to IIa group, IIIa group, and lanthanum series,

and wherein each of B1, B2,⋯, Bn is an element selected so as to be different from one another from a group consisting of Ti, Nb, Ta, Zr, Hf, Y.

[0013] Also, in accordance with characteristics of the present invention, there is provided a method of manufacturing the ferroelectric memory device defined in claim 7, the method comprises the steps of:

providing the ferroelectric layer by carrying out a step (d) after forming an amorphous layer having a desired thickness by carrying out steps (a) to (c) for one of once and predetermined times,

(a) coating mixed-metal alkoxide composed of Sr, Ta, and Nb which being dissolved in a solvent on a base substance,

(b) evaporating the solvent,

(c) removing organic elements by heat treatment,

(d) carrying out annealing for crystallization at a temperature above a temperature to be crystallized.

[0014] While the novel features of the invention are set forth in a general fashion, both as to organization and content, the invention will be better understood and appreciated, along with other objects and features thereof, from the following detailed description taken in conjunction with the drawings.

Brief description of the drawings

[0015]

Fig. 1 is a view showing a construction of an FET 20 having an MFMIS structure which forms a ferroelectric memory device in an embodiment of the present invention.

Fig. 2 is a diagram showing an equivalent circuit of the FET 20 during the writing.

Fig. 3 is a graph showing a relationship between thicknesses tf of a ferroelectric layer 28 and electric fields Ef applied to a capacitor Cf.

Fig. 4A is a graph being drawn according to plots showing a relationship between k1 and k2 of major ferroelectric substances.

Fig. 4B is an enlarged view of an area (z) of the graph shown in Fig. 4A.

Fig. 5 is a graph showing x-ray diffraction patterns of a memory device being fabricated.

Fig. 6 is a table showing both crystallographical and electric characteristics of $Sr_nNb_2O_7$ and $Sr_2Ta_2O_7$.

Fig. 7 is a graph showing a relationship between mixture ratios x of Nb in a mixed crystal $Sr_2(Ta_{1-x}Nb_x)_2O_7$ and curie temperature Tc of the mixed crystal.

Fig. 8 is a graph showing the x-ray diffraction patterns of the memory device having a ratio x of 0.3.

Fig. 9 is a graph showing a relationship between voltages applied to a thin film made of $Sr_2(Ta_{1-x}Nb_x)_2O_7$ and polarization states generated therein.

Fig. 10 is a graph showing a relationship between bias voltages applied to the thin film of $Sr_2(Ta_{1-x}Nb_x)_2O_7$ and capacitances thereof.

Fig. 11 is a graph showing leakage current characteristics of the thin film of $Sr_2(Ta_{1-x}Nb_x)_2O_7$.

Fig. 12A is a view showing a structure of an FET in another embodiment of the present invention.

Fig. 12B is a view showing a structure of an FET in far another embodiment of the present invention.

Fig. 12C is a view showing a structure of an FET in still another embodiment of the present invention.

Fig. 13 is a view of an FET using the conventional ferroelectric layer.

The best mode of preferred embodiment to carry out the present invention

[0016] A view showing a construction of an FET 20 having an MFMIS structure which forms a ferroelectric memory device in an embodiment of the present invention is depicted in Fig. 1. The FET 20 comprises a source region S and a drain region D, both formed in a semiconductor substrate 22 made of silicon. A channel region CH is formed between the source region S and the drain region D.

[0017] A gate oxidation layer 24 acts as an insulation layer is formed on the channel region CH. The gate oxidation layer 24 is made of SiO_2. A floating gate 26 forming a lower conductive layer is formed on the gate oxidation layer 24. The floating gate 26 has a stacked structure of Pt/IrO_2.

[0018] On the floating gate 26, a ferroelectric layer 28 described later is disposed. A control gate 30 acts as an upper conductive layer is formed on the ferroelectric layer 28. The control gate 30 is made of Pt.

[0019] Next, an equivalent circuit of the FET 20 during the writing is diagrammed in Fig. 2. The equivalent circuit of the FET 20 during the writing is in a formation of connecting a capacitor Cf (capacity Cf) which includes the ferroelectric layer 28 and a capacitor Cox (capacity Cox) having the gate oxidation layer 24 in series. Under the circumstances, a divided voltage Vf defined by the following equation is applied to the capacitor Cf when a voltage (equal to either of +V or -V) is applied at a point located between the substrate 22 and the control gate

30,

$$Vf=Cox/(Cf+Cox) \cdot V.$$

[0020] An electric field Ef applied to the capacitor Cf is defined as the following expression when the area of the capacitor Cf and that of the capacitor Cox is set as the same with each other,

$$Ef=\epsilon ox/(\epsilon f \cdot tox+\epsilon ox \cdot tf) \cdot V \quad (1)$$

wherein ϵf is a relative dielectric constant of a ferroelectric substance, ϵox represents a relative dielectric constant of SiO_2, tf is a thickness of the ferroelectric layer, and tox represents a thickness of the gate oxidation layer.

[0021] In order to cause a polarization reversal in the opposite polarity within the ferroelectric layer 28, the following expression must be satisfied, $Ef>\alpha Ec$ (2) wherein αEc represents an electric field required for causing a polarization reversal, α is a constant, and Ec represents coercive field.

[0022] The following expression is obtained according to the expressions (1) and (2),

$$\epsilon ox/(\epsilon f \cdot tox+\epsilon ox \cdot tf) \cdot V>\alpha Ec \quad (3)$$

[0023] In order to increase the value of the left member of the expression (3) that is the electric field Ef applied to the capacitor Cf, either ways of decreasing the relative dielectric constant ϵf or making the thickness tf of the ferroelectric layer 28 and/or the thickness tox of the gate oxidation layer 24 thinner should be taken. However, there is a limitation of making the thickness tox of the gate oxidation layer 4 thinner.

[0024] Fig. 3 is a graph showing a relationship between thicknesses tf of a ferroelectric layer 28 and electric fields Ef applied to the capacitor Cf when the thickness tox of the gate oxidation layer 24 is fixed to 10nm as well as using voltages V applied at a point located between the substrate 22 and the control gate 30 as a parameter. Solid curves show the relationship when the relative dielectric constant ϵf of the ferroelectric substance is 10, dashed curves illustrate the relationship when the relative dielectric constant ϵf of the ferroelectric substance is 100.

[0025] As it is understood from Fig. 3, no significant increase of the electric fields Ef is observed when the relative dielectric constant ϵf of the ferroelectric substance is 100 even if the thickness tf of the ferroelectric layer 28 is made thinner. On the contrary, significant increase of the electric fields Ef is observed when the relative dielectric constant ϵf of the ferroelectric substance is 10 in the case of making the thickness tf of the ferroelectric layer 28 thinner. In other words, it is necessary to make the thickness tf of the ferroelectric layer 28 thinner while decreasing the relative dielectric constant ϵf in order to increase the electric fields Ef.

[0026] The expression (3) may be formulized in another expression shown in below,

$$V/\alpha>Ec \cdot \epsilon f/\epsilon ox \cdot tox+tf=k1 \quad (4).$$

[0027] In order to cause a polarization reversal in the opposite polarity within the ferroelectric layer 28, the expression (4) must be satisfied.

[0028] Next, electric fields Eox being generated in accordance with a divided voltage Vox applied to a capacitor Cox including the gate oxidation layer 24 can be defined by the following expression,

$$Eox=\epsilon f/\epsilon ox \cdot Ef.$$

[0029] The expression shown in above may be expressed as below when the electric field αEc representing the electric field required for causing the polarization reversal is applied to the capacitor Cf as the electric field Ef,

$$Eox=\epsilon f/\epsilon ox \cdot \alpha Ec \quad (5).$$

[0030] On the other hand, in order to prevent dielectric breakdown of the gate oxidation 24, the following expression must be satisfied,

$$Eox<Ebd \quad (6)$$

wherein Ebd represents strength of the dielectric breakdown of the gate oxidation layer 24.

[0031] The following expression is obtained according to the expressions (5) and (6),

$$Ebd \cdot \epsilon ox/\alpha>Ec \cdot \epsilon f=k2 \quad (7).$$

[0032] In order words, the expression (7) shown in above must be satisfied in order to prevent dielectric breakdown of the gate oxidation layer 24.

[0033] Fig. 4A is a graph being drawn according to plots showing a relationship between k1 used in the expression (4) and k2 used in the expression (7) of major ferroelectric substances. In the graph, some of the values used in these expressions are defined as the followings,

tox=15nm,
ϵox=3.9, and
tf=200nm.

[0034] Another expression shown in below is introduced according to the expression (4),

$$2.5[v]>k1 \text{ when} \quad (8),$$

values used in the expressions are defined as below,

V=5.0V,

α=2,
Ebd=8MV/cm, and
ϵox=3.9.

[0035] Further, another expression is defined as below according to the expression (7),

$$1.56X10^{9}\ [V/m]>k2 \qquad (9).$$

[0036] Both the expressions (8) and (9) need to be satisfied in order to cause the polarization reversal of the ferroelectric layer 28 as well as preventing the dielectric breakdown of the gate oxidation layer 24.

[0037] The ferroelectric substances, these located in an area (z) illustrated with a dot line shown in Fig. 4A satisfy the requirements stated in above. Fig. 4B is an enlarged view illustrating the vicinity of the area (z).

[0038] Further, in order to form the source S and the drain D shown in Fig. 1 by means of self aligning, thermal diffusion of implanted impurities need to be carried out, the impurities being implanted using the ferroelectric layer 28 as a mask after forming the ferroelectric layer 28. Therefore, the ferroelectric layer 28 should be composed of a ferroelectric substance having a high melting point which withstands heat treatments carried out in the vicinity of 800°C.

[0039] Within a various ferroelectric substances, $Sr_2Nb_2O_7$ is selected as a ferroelectric substance which qualities the requirements described in above. A thin film made of $Sr_2Nb_2O_7$ is formed using the Sol-Gel method described later. Fig. 5 is a graph showing x-ray diffraction patterns of a memory device being fabricated using annealing temperatures for crystallization as a parameter. As clearly be recognized from Fig. 5, the peaks show unique characteristics of $Sr_2Nb_2O_7$ appeared on the graph when the annealing temperature is equal to or more 900°C, so that, it is understood that $Sr_2Nb_2O_7$ is in crystallization.

[0040] Relative dielectric constant ϵf of the thin film made of $Sr_2Nb_2O_7$ thus obtained is measured as the vicinity of 45. It is, however, not possible to confirm ferroelectricity (hysteresis characteristics between the voltage applied thereto and the polarization therein) of the film. A curie temperature Tc of the thin film is considered as one of the reasons. Curie temperature is a temperature located at the boundary between temperatures in which a substance indicates ferroelectricity and temperatures in which the substance shows dielectricity. In this connection, the substance indicates ferroelectricity when the temperature of the substance is lower than its curie temperature. It is expected that the thin film made of $Sr_2Nb_2O_7$ shows ferroelectricity in the room temperature according to a principle of crystallographical because the curie temperature Tc of $Sr_2Nb_2O_7$ is at 1342°C.

[0041] However, no vibrations of their lattices are observed (the phenomena is called as "suspension of the soft mode") at the room temperature. It is considered that its high curie temperature prevent the thin film from the vibrations, so that no ferroelectricity is observed at the room temperature. The inventors focus attention on $Sr_2Ta_2O_7$ having the same crystalline structure as that of $Sr_2Nb_2O_7$ and a remarkably lower curie temperature (TC= -107°C).

[0042] Crystallographical and electric characteristics of $Sr_2Nb_2O_7$ and $Sr_2Ta_2O_7$ are listed on a table shown in Fig. 6. The crystal structure of $Sr_2Nb_2O_7$ and $Sr_2Ta_2O_7$ (both of which have pyramid quadratic structure) is similar to each other. Under the fact, the inventors make a thin film using a mixed crystal made of $Sr_2Nb_2O_7$ and $Sr_2Ta_2O_7$ which satisfies the following condition in experimental basis, that is expressed as the following,

$$Sr_2(Ta_{1-x}Nb_x)_2O_7 \qquad (10),$$

wherein 0<x<1.

[0043] The mixed crystal consist of $Sr_2(Ta_{1-x}Nb_x)_2O_7$ changes its crystallographical and electric characteristics consecutively correspond to its mixture ratio. Fig. 7 is a graph showing a relationship between mixture ratios x of Nb in a mixed crystal $Sr_2(Ta_{1-x}Nb_x)_2O_7$ and a curie temperature of the mixed crystal. It is understood that the mixture ratio x of Nb in the mixed crystal should be xl in order to obtain a curie temperature of Tcl according to the graph.

[0044] Mixed crystals composed of the substance shown in the expression (10) under a plurality of mixture ratio x such as 0.1, 0.2, 0.3, 0.4, and 0.6 are made respectively. Sol-Gel method is used for forming a thin film made of the mixed crystal. Processes for forming a thin film made of the mixed crystal under Sol-Gel method will be described hereunder.

[0045] At first, mixed-metal alkoxide composed of Sr, Ta, and Nb, which is dissolved in a solvent is prepared, and the alkoxide thus dissolved is coated on a base substance (this substance becoming the floating gate 26 as a result of patterning, see Fig. 1) having a stacked structure of Pt/IrO_2. In this embodiment, 2-metoxyethernol is used for the solvent. The alkoxide is coated by spin coating method.

[0046] The solvent is evaporated at a temperature of 180°C.

[0047] Thereafter, in order to remove organic elements, heat treatment using dry air heated at 400°C is carried out for 30 minutes.

[0048] Amorphous layer having a predetermined thickness is formed by carrying out these processes repeatedly. In this embodiment, the processes described above are carried out for a total of four times (four coatings). It is not necessary to repeat the processes as described above, the processes may be carried out just once when the predetermined thickness is much thinner than that of above.

[0049] Next, annealing for crystallization is carried out to the amorphous layer thus formed. The annealing in

this embodiment is carried out by rapid thermal annealing (RTA) method. That is, heat treatment using O_2 within a range of 850 to 1000°C is carried out for 1 minutes. Thus, the thin film made of the mixed crystal composed of the substance shown in the expression (10) is obtained. The thickness tf of the thin film thus obtained is 145nm.

[0050] Although, various temperatures, durations, and other conditions are described above, the present invention is not limited to the conditions, alternative conditions can be used.

[0051] Also, the method for forming the thin film made of the mixed crystal composed of $Sr_2(Ta_{1-x}Nb_x)_2O_7$ is not limited to Sol-Gel method. Other available methods conventionally used such as spattering method, MOCVD method, MOD method, IBS method, PLD method, and the like can be used for forming the thin film.

[0052] Another layer made of Pt (this layer becoming the control gate 30 as a result of patterning, see Fig. 1) is disposed on the thin film thus obtained by carrying out spattering method.

[0053] Fig. 8 is a graph showing the x-ray diffraction patterns of the memory device having a ratio x of 0.3 using the annealing temperatures for crystallization as a parameter. As it is understood from Fig. 8, the peaks show unique characteristics of $Sr_2(Ta_{1-x}Nb_x)_2O_7$ appeared on the graph when the annealing temperature is equal to or more 950°C, so that, it is understood that $Sr_2(Ta_{1-x}Nb_x)_2O_7$ is in crystallization. In our observation, the surface of the thin film made of $Sr_2(Ta_{1-x}Nb_x)_2O_7$ was very smooth and fine structure in crystallization.

[0054] The peaks showing unique characteristics of $Sr_2(Ta_{1-x}Nb_x)_2O_7$ are not observed in the graph when the annealing temperatures are respectively in 850°C and 900°C. Instead of these peaks, other peaks indicating that the substance is in $Sr_2(Ta_{1-x}Nb_x)_{10}O_{27}$ shown in the graph are observed. In our experiment, a relationship between the x-ray diffraction patterns of the memory device and the annealing temperatures are not depending on the values of x within a range of $0.1 \leq x \leq 0.6$.

[0055] Fig. 9 is a graph showing a relationship between voltages applied to the thin film made of $Sr_2(Ta_{1-x}Nb_x)_2O_7$ and polarization states generated therein using the value x as a parameter. The relationship between the voltages and the polarization states is measured with a Sawyer tower circuit using a frequency of 1KHz. The axis of abscissas shows the voltages, and the axis of ordinates represents the polarization states. The relationship between the voltages and the polarization states shows hysteresis characteristics when the values of x is in a range of $0.1 \leq x \leq 0.3$. According to Fig. 7, it is understood that curie temperature Tc of the thin film is in a range of 180°C to 600°C when the values of x are in a range of $0.1 \leq x \leq 0.3$ (As in Fig. 7, curie temperatures Tc of the thin film are either in the vicinity of 410°C or 520°C when the values of x are in 0.2 and 0.3 respectively).

[0056] On the contrary, no hysteresis characteristics are shown when the values of x are in both 0.4 and 0.6 (not shown). The phenomena might be caused due to high curie temperature Tc (As in Fig. 7, curie temperatures Tc of the thin film are either in the vicinity of 735°C or 1000°C when the values of x are in 0.4 and 0.6 respectively).

[0057] It is not preferable to set the value of x in an excessively small value because it leads undesirable decrease of curie temperature Tc. As it is understood from Fig. 9, remanent polarization Pr is in the largest value such as 0.5μc/cm^2 when the values of x is in 0.3. At that time, coercive field Ec was measured at 44KV/cm.

[0058] Fig. 10 is a graph showing a relationship between bias voltages applied to the thin film of $Sr_2(Ta_{1-x}Nb_x)_2O_7$ and capacitances thereof using the value x as a parameter. The relationship between the voltages and the capacitances is measured with an LCR meter generating 25mV and 100 KHz (model No. HP4284A). The axis of abscissas shows the bias voltages, and the axis of ordinates represents the capacitances. Sweep rate of the measurement was 0.5V/second. It is clearly understood that the thin film being formed shows hysteresis characteristics when the values of x is in a range of $0.1 \leq x \leq 0.3$.

[0059] Relative dielectric constant ϵr of the thin film was 53 when the value x is 0.3, the dielectric constant being calculated from the capacitance when 0V is applied thereto as the bias voltage.

[0060] Fig. 11 is a graph showing leakage currents of the thin film made of $Sr_2(Ta_{1-x}Nb_x)_2O_7$ using the value x as a parameter. The axis of abscissas shows the voltages, and the axis of ordinates represents density of the leakage currents. The density of the leakage currents is the highest value when the value x is 0.3, and it becomes the lowest value when the value x is 0.1. The results might be caused by measurement error. In any case, these leakage current density is a relatively small value such as equal or less than $6X10^{-7}$A/cm^2 when a voltage 3V (in electric field equivalent of approximately 200KV/cm) is applied to the thin film.

[0061] Although, $Sr_2(Ta_{1-x}Nb_x)_2O_7$ is used as an example of the mixed crystal which can express as $(A1_{y1}A2_{y2} \cdots An_{yn})_2(B1_{x1}B2_{x2} \cdots Bm_{xm})_2O_7$ in the embodiments described above, the substance used for forming the thin film to realize the present invention is not limited to $Sr_2(Ta_{1-x}Nb_x)_2O_7$. For example, elements belong to IIa group, IIIa group, and lanthanum series may be used as A1, A2,⋯An of the mixed crystal expressed as $(A1_{y1}A2_{y2} \cdots An_{yn})_2(B1_{x1}B2_{x2} \cdots Bm_{xm})_2O_7$.

[0062] As the elements belong to IIa group, Mg, Ca, Ba and the like may be used in addition to Sr. As the elements belong to IIIa group, Sc, Y, La, Ac and the like can be used. Further, as the elements belong to lanthanum

series, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, La and the like may be used.

[0063] In addition to Nb and Ta, for example Ti, Zr, Hf, Y and the like may also be used as B1,B2···Bm of the mixed crystal expressed as $(A1_{y1}A2_{y2}\cdots An_{yn})_2(B1_{x1}B2_{x2}\cdots Bm_{xm})_2O_7$.

[0064] In other words, the thin film can also be formed using mixed crystals composed any of $Ca_2Nb_2O_7$, $La_2Ti_2O_7$, $Ce_2Ti_2O_7$, $Pr_2Ti_2O_7$, $Nd_2Ti_2O_7$, $Sm_2Ti_2O_7$, $Gd_2Ti_2O_7$, $Y_2Ti_2O_7$ and the like in addition to $Sr_2Nb_2O_7$ and $Sr_2Ta_2O_7$.

[0065] Although, the thin film made of mixed crystal is designed so that curie temperature Tc of which is in a range of 180°C≤x≤600°C in the embodiments described above, curie temperature of the thin film used in the present invention is not limited to the temperature range. A ferroelectric thin film having desired curie temperature Tc corresponding to the temperature at which the device being in operation is preferred.

[0066] Though, the ferroelectric thin film according to the present invention is applied to the FET 20 having the MFMIS structure in the embodiments described above, the application of the present invention is not limited to the FET having the structure. The present invention may also be applicable to FETs having other structures, such as any of the FET 40 having MFIS structure shown in Fig. 12A, the FET 50 having the MIFIS structure shown in Fig. 12B, and the FET 60 having the MFS structure shown in Fig. 12C.

[0067] The FET 40 having the MFIS structure is considered as an equivalent circuit in which a capacitor including an insulation layer 42, another capacitor which comprises a ferroelectric layer 44 is connected in series during the writing. The FET 50 having the MIFIS structure may also be considered as an equivalent circuit having a formation of connecting a capacitor which includes an insulation layer 52, another capacitor which comprises a ferroelectric layer 54, and still another capacitor which includes an insulation layer 56 in series during the writing.

[0068] The FET 60 having the MFS structure further be considered as an equivalent circuit in which a capacitor including an insulation layer 62 and another capacitor which comprises a ferroelectric layer 64 is connected in series during the writing. The insulation layer 62 made of SiO_2 is formed unintentionally during a process of depositing the ferroelectric layer 64 on a semiconductor substrate 61 of silicon.

[0069] The application of the present invention is not limited to FETs including a ferroelectric layer. The present invention may also be applicable to other types of memory devices including a first capacitor having a ferroelectric layer and a second capacitor substantially connected to the first capacitor in series. In addition, the present invention is applicable generally to memory devices including a ferroelectric material.

[0070] The ferroelectric memory device in accordance with the present invention is characterized in that, a ferroelectric memory device includes a ferroelectric layer in which information being stored using its hysteresis characteristics, and the ferroelectric layer is composed of a mixed crystal defined by expressions of;

$(A1_{y1}A2_{y2}\cdots An_{yn})_2(B1_{x1}B2_{x2}\cdots Bm_{xm})_2O_7$,
and $x1+x2+\cdots+xm=1$,
and $y1+y2+\cdots+yn=1$,
and each of $x1, x2, \cdots xm$, $y1, y2, \cdots yn$ has a value equal to or greater than 0, and equal to or less than 1,
and at least two of $x1, x2, \cdots xm$, $y1, y2, \cdots yn$ have values greater than 0, and less than 1,
and each of A1, A2,···, An is an element selected so as to be different from one another from a group consisting of elements belong to IIa group, IIIa group, and lanthanum series,
and each of B1, B2,···, Bn is an element selected so as to be different from one another from a group consisting of Ti, Nb, Ta, Zr, Hf, Y.

[0071] It is, therefore, dielectric constant of the ferroelectric layer can be reduced by composing the ferroelectric layer with an $A_2B_2O_7$ type crystal. Also, the melting point of the ferroelectric layer may be increased. Further, characteristic values of the ferroelectric layer such as curie temperature related with ferroelectricity thereof can be controlled as desired by composing the layer with a mixed crystal. In this way, a ferroelectric layer having characteristics of desired ferroelectricity, a low dielectric constant, and a high melting point may be obtained.

[0072] Also, the ferroelectric memory device in accordance with the present invention is characterized in that, curie temperature Tc of the ferroelectric layer is in a range of about 180°C to about 600°C. In this way, a ferroelectric layer which shows stable ferroelectricity within an operating range of -50°C to +150°C can be obtained.

[0073] Further, the ferroelectric memory device in accordance with the present invention is characterized in that, curie temperature Tc of the ferroelectric layer is in a range of about 500°C to about 600°C. In this way, a ferroelectric layer which shows much stable ferroelectricity can be obtained.

[0074] The ferroelectric memory device in accordance with the present invention is characterized in that, the ferroelectric memory device includes a first capacitor having the ferroelectric layer, and a second capacitor connected to the first capacitor substantially in series, and information is stored in accordance with a divided voltage applied to the ferroelectric layer of the first capacitor by applying a voltage which corresponds to the information to be stored to both ends of the first capacitor and the second capacitor connected in series.

[0075] In other words, the information is stored in accordance with the divided voltage applied to the ferroelectric layer of the first capacitor by applying a voltage

corresponds to the information to be stored to both ends of the first capacitor and the second capacitor connected in series.

[0076] It is, therefore, the divided voltage applied to the first capacitor can be increased using a ferroelectric layer having a low dielectric constant. In this way, polarization reversal of the ferroelectric layer can be caused easily during the writing. As a result, storing information into the ferroelectric memory device can be carried out easily.

[0077] Also, the ferroelectric memory device in accordance with the present invention is characterized in that, the ferroelectric memory device comprises, a source region, a drain region, a channel region formed between the source region and the drain region, a substantially insulation layer disposed on the channel region, a ferroelectric layer disposed above the substantially insulation layer, and an upper conductive layer disposed on the ferroelectric layer.

[0078] Therefore, the probability of lattice defects in a ferroelectric layer once formed is decreased in an FET requiring heat treatment after forming the ferroelectric layer by using the ferroelectric layer having a high melting point. In this way, it is possible to obtain a ferroelectric memory device with high reliability.

[0079] Further, the ferroelectric memory device in accordance with the present invention is characterized in that, the ferroelectric memory device has a lower conductive layer between the substantially insulation layer and the ferroelectric layer. In this way, it is possible to obtain a ferroelectric memory device with much high reliability by fabricating it with a structure so called MFMIS (Metal Ferroelectric Metal Insulator Silicon).

[0080] The ferroelectric memory device in accordance with the present invention is characterized in that, the ferroelectric layer is composed of a mixed crystal defined by expressions of;

$Sr_2(Ta_{1-x}NB_x)_2O_7$,
and the value of x is $0<x<1$.

[0081] Consequently, a ferroelectric layer which shows ferroelectricity at a desired temperature range can be formed easily using a mixed crystal composed of $Sr_2Nb_2O_7$ indicating a high curie temperature Tc and $Sr_2Ta_2O_7$ having a low curie temperature Tc.

[0082] Also, the ferroelectric memory device in accordance with the present invention is characterized in that, the value of x is in a range of about 0.1 to about 0.3. It is, therefore, possible to form a ferroelectric layer which shows ferroelectricity at the room temperature by controlling a mixture ratio of the mixed crystal within the range.

[0083] Further, the ferroelectric memory device in accordance with the present invention is characterized in that, the value of x is about 0.3. It is, therefore, possible to form a ferroelectric layer which shows much higher ferroelectricity at the room temperature by controlling a mixture ratio of the mixed crystal to the value.

[0084] The method of manufacturing a ferroelectric memory device in accordance with the present invention is characterized in that, the method comprises the steps of:

providing the ferroelectric layer by carrying out a step (d) after forming an amorphous layer having a desired thickness by carrying out steps (a) to (c) for one of once and predetermined times,

(a) coating mixed-metal alkoxide composed of Sr, Ta, and Nb which being dissolved in a solvent on a base substance,
(b) evaporating the solvent,
(c) removing organic elements by heat treatment,
(d) carrying out annealing for crystallization at a temperature above a temperature to be crystallized. In this way, a ferroelectric layer having characteristics of a low dielectric constant, a high melting point, and desired ferroelectricity can be formed in a desired thickness.

[0085] While the invention has been described in its preferred embodiments, it is to be understood that the words which have been used are words of description rather than limitation and that changes within the purview of the appended claims can be made without departing from the true scope and spirit of the invention in its broader aspects.

Claims

1. A ferroelectric memory device including a ferroelectric layer in which information being stored using its hysteresis characteristics, wherein the ferroelectric layer is composed of a mixed crystal defined by expressions of;

$(A1_{y1}A2_{y2}\cdots An_{yn})_2(B1_{x1}B2_{x2}\ldots Bm_{xm})_2O_7$,
and wherein $x1+x2+\cdots+xm=1$,
and wherein $y1+y2+\cdots+yn=1$,
and wherein each of $x1,x2,\cdots xm$, $y1,y2,\cdots yn$ has a value equal to or greater than 0, and equal to or less than 1,
and wherein at least two of $x1,x2,\cdots xm$, $y1,y2,\cdots yn$ have values greater than 0, and less than 1,
and wherein each of A1, A2,···, An is an element selected so as to be different from one another from a group consisting of elements belong to IIa group, IIIa group, and lanthanum series,
and wherein each of B1, B2,···, Bn is an element selected so as to be different from one another from a group consisting of Ti, Nb, Ta, Zr, Hf, Y.

2. The ferroelectric memory device in accordance with claim 1, wherein curie temperature Tc of the ferroelectric layer is in a range of about 180°C to about 600°C.

3. The ferroelectric memory device in accordance with claim 2, wherein curie temperature Tc of the ferroelectric layer is in a range of about 500°C to about 600°C.

4. The ferroelectric memory device in accordance with claim 1, wherein the ferroelectric memory device includes a first capacitor having the ferroelectric layer, and a second capacitor connected to the first capacitor substantially in series,
and wherein information is stored in accordance with a divided voltage applied to the ferroelectric layer of the first capacitor by applying a voltage which corresponds to the information to be stored to both ends of the first capacitor and the second capacitor connected in series.

5. The ferroelectric memory device in accordance with claim 4, wherein the ferroelectric memory device comprises,

a source region,
a drain region,
a channel region formed between the source region and the drain region,
a substantially insulation layer disposed on the channel region,
a ferroelectric layer disposed above the substantially insulation layer, and
an upper conductive layer disposed on the ferroelectric layer.

6. The ferroelectric memory device in accordance with claim 5, wherein the ferroelectric memory device has a lower conductive layer between the substantially insulation layer and the ferroelectric layer.

7. The ferroelectric memory device in accordance with claim 1, wherein the ferroelectric layer is composed of a mixed crystal defined by expressions of;

$Sr_2 (Ta_{1-x}NB_x)_2 0_7$,
and wherein the value of x is $0<x<1$.

8. The ferroelectric memory device in accordance with claim 7, wherein the value of x is in a range of about 0.1 to about 0.3.

9. The ferroelectric memory device in accordance with claim 8, wherein the value of x is about 0.3.

10. The ferroelectric memory device in accordance with claim 7, wherein curie temperature Tc of the ferroelectric layer is in a range of about 180°C to about 600°C.

11. The ferroelectric memory device in accordance with claim 10, wherein curie temperature Tc of the ferroelectric layer is in a range of about 500°C to about 600°C.

12. The ferroelectric memory device in accordance with claim 7, wherein the ferroelectric memory device includes a first capacitor having the ferroelectric layer, and a second capacitor connected to the first capacitor substantially in series,
and wherein information is stored in accordance with a divided voltage applied to the ferroelectric layer of the first capacitor by applying a voltage which corresponds to the information to be stored to both ends of the first capacitor and the second capacitor connected in series.

13. The ferroelectric memory device in accordance with claim 12, wherein the ferroelectric memory device comprises,

a source region,
a drain region,
a channel region formed between the source region and the drain region,
a substantially insulation layer disposed on the channel region,
a ferroelectric layer disposed above the substantially insulation layer, and
an upper conductive layer disposed on the ferroelectric layer.

14. The ferroelectric memory device in accordance with claim 13, wherein the ferroelectric memory device has a lower conductive layer between the substantially insulation layer and the ferroelectric layer.

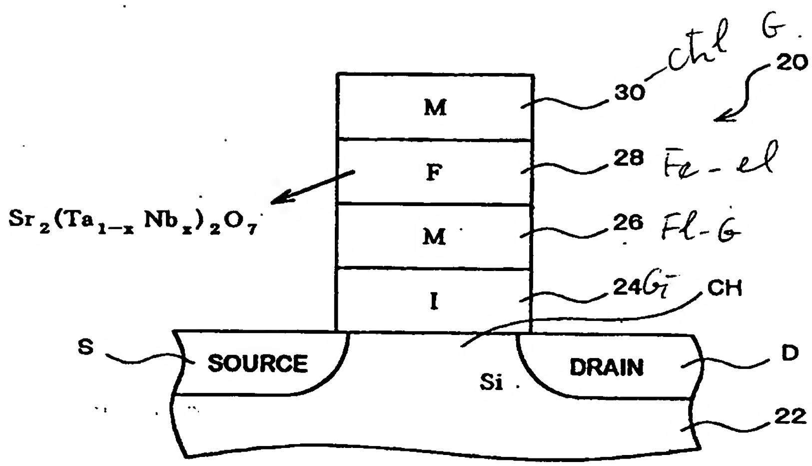
15. A method of manufacturing the ferroelectric memory device defined in claim 7, the method comprising the steps of:

providing the ferroelectric layer by carrying out a step (d) after forming an amorphous layer having a desired thickness by carrying out steps (a) to (c) for one of once and predetermined times,

(a) coating mixed-metal alkoxide composed of Sr, Ta, and Nb which being dissolved in a solvent on a base substance,
(b) evaporating the solvent,
(c) removing organic elements by heat treatment,
(d) carrying out annealing for crystallization at a temperature above a temperature

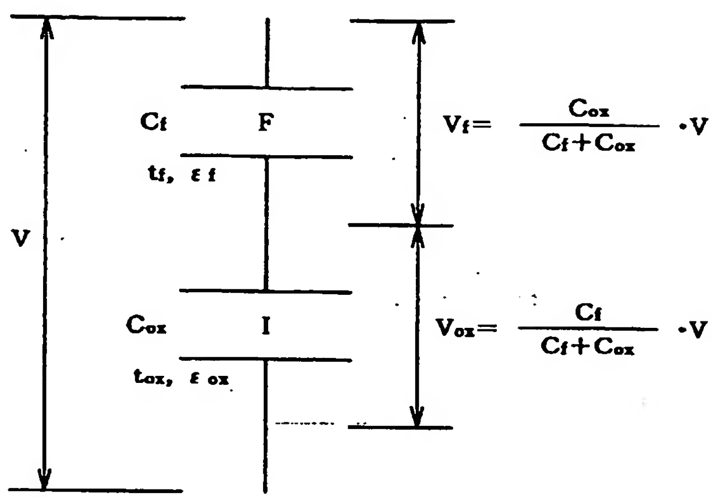
to be crystallized.

FIG.1



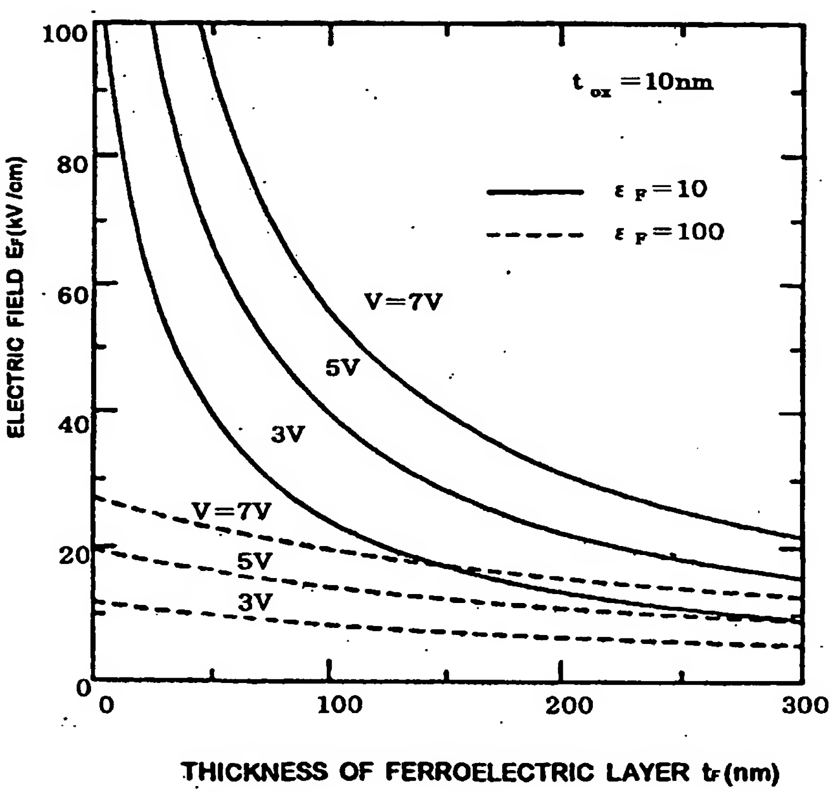
20:FET
22:SILICON SEMICONDUCTOR SUBSTRATE
24:GATE OXIDATION LAYER
26:FLOATING GATE
28:FERROELECTRIC LAYER
30:CONTROL GATE
CH:CHANNEL REGION

FIG.2



C_f
F
$t_f,\ \varepsilon_f$
V
C_{ox}
I
$t_{ox},\ \varepsilon_{ox}$
$V_f = \dfrac{C_{ox}}{C_f + C_{ox}} \cdot V$
$V_{ox} = \dfrac{C_f}{C_f + C_{ox}} \cdot V$

FIG.3



100
80
60
40
20
0
0
100
200
300
ELECTRIC FIELD E_F(kV/cm)
THICKNESS OF FERROELECTRIC LAYER t_F(nm)
t_{ox} =10nm
ε_F=10
ε_F=100
V=7V
5V
3V
V=7V
5V
3V

FIG.4A

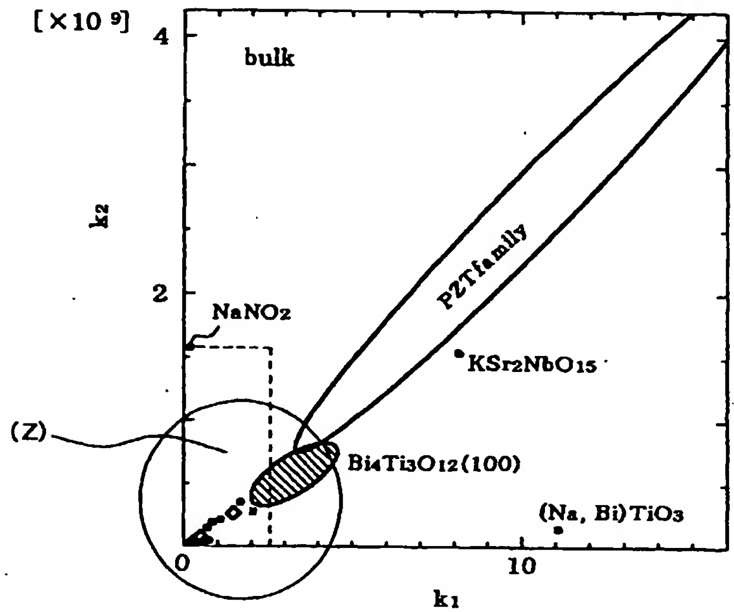

[×10 9]
4
bulk
k2
2
NaNO2
(Z)
PZT family
KSr2NbO15
Bi4Ti3O12(100)
(Na, Bi)TiO3
0
10
k1

FIG.4B

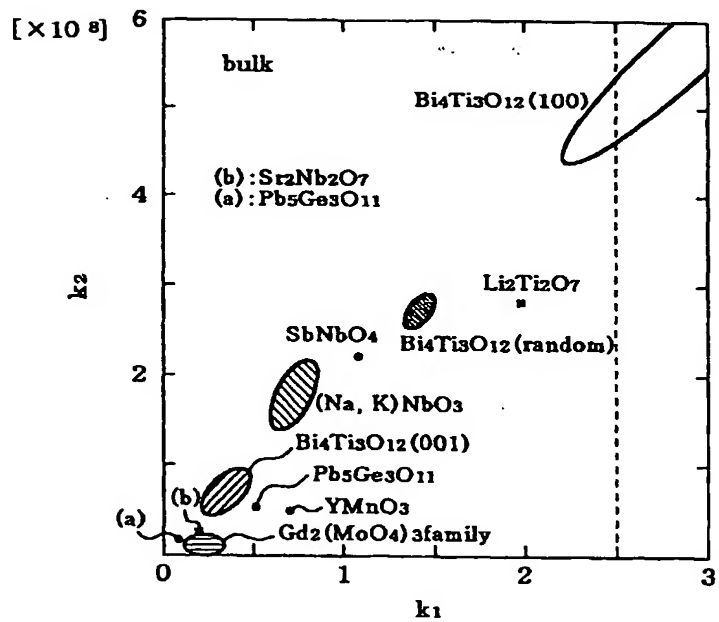

[×10 8]
6
bulk
Bi4Ti3O12(100)
(b):Sr2Nb2O7
(a):Pb5Ge3O11
4
k2
Li2Ti2O7
SbNbO4
Bi4Ti3O12(random)
2
(Na, K)NbO3
Bi4Ti3O12(001)
Pb5Ge3O11
(b)
YMnO3
(a)
Gd2(MoO4)3family
0
1
2
3
k1

FIG.5

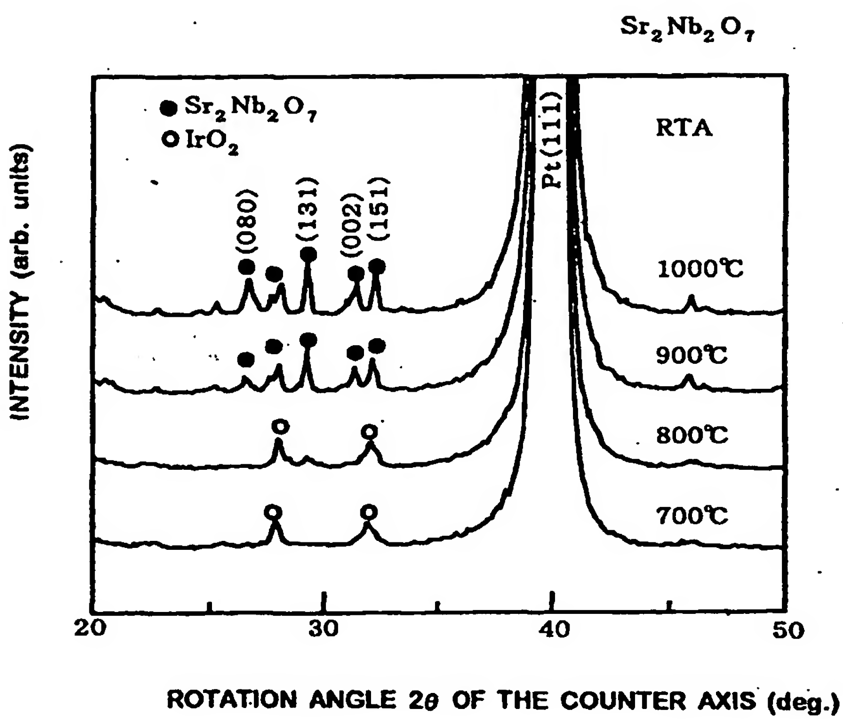

$Sr_2Nb_2O_7$
● $Sr_2Nb_2O_7$
○ IrO_2
INTENSITY (arb. units)
(080)
(131)
(002)
(151)
Pt(111)
RTA
1000℃
900℃
800℃
700℃
20
30
40
50
ROTATION ANGLE 2θ OF THE COUNTER AXIS (deg.)

FIG.6

		$Sr_2Nb_2O_7$	$Sr_2Ta_2O_7$
CRYSTAL STRUCTURE		PYRAMID QUADRATIC	PYRAMID QUADRATIC
LATTICE CONSTANT	a(Å)	3. 993	3. 937
LATTICE CONSTANT	b(Å)	26. 726	27. 198
LATTICE CONSTANT	c(Å)	5. 683	5. 692
MELTING POINT	T_m(℃)	1700	2000
CURIE TEMPERATURE	T_c(℃)	1342	−107
REMANENT POLARIZATION	$P_r(\mu C/cm^2)$	9	1. 9 [a)]
COERCIVE FIELD	E_c(kV/cm)	6	0. 4 [a)]
RELATIVE DIELECTRIC CONSTANT	ε_a	75	37
RELATIVE DIELECTRIC CONSTANT	ε_b	46	22
RELATIVE DIELECTRIC CONSTANT	ε_c	43	644

CRYSTALLOGRAPHIC AND ELECTRIC CHARACTERISTICS OF $Sr_2Nb_2O_7$, $Sr_2Ta_2O_7$

a) AT A TEMPERATURE OF LIQUID NITROGEN

FIG.7

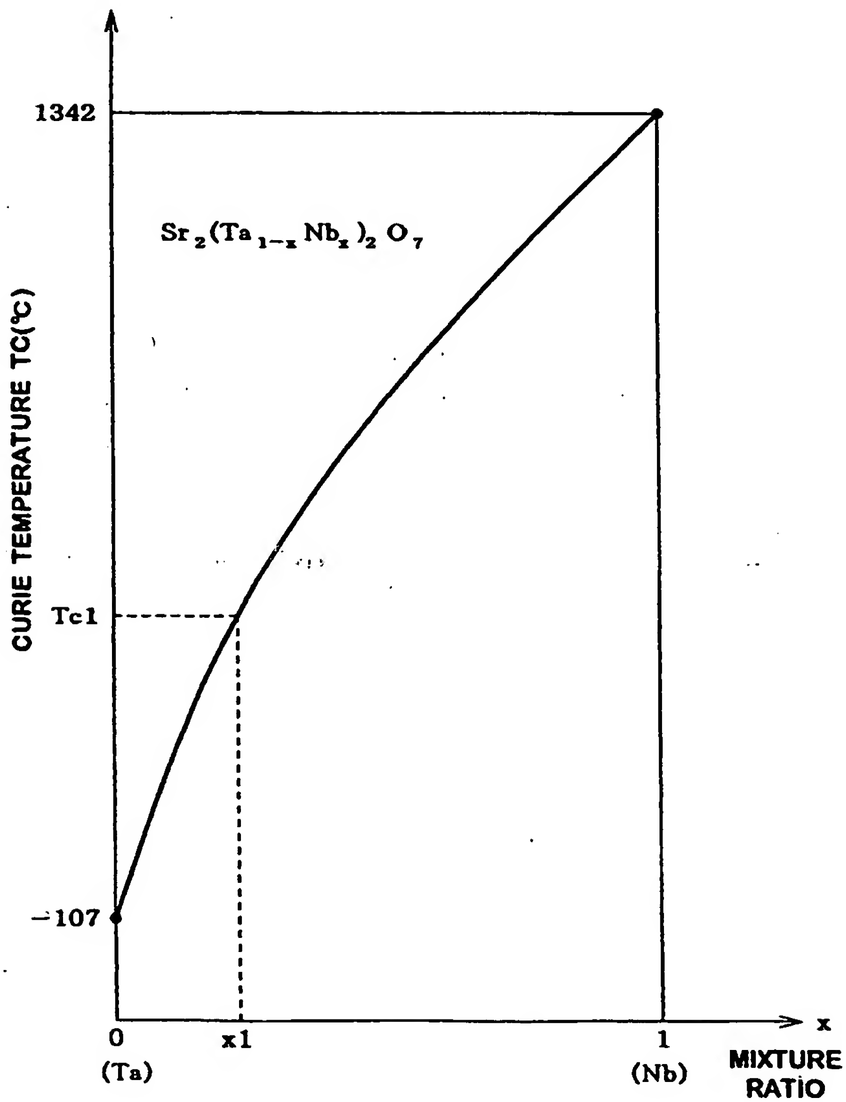

1342
$Sr_2(Ta_{1-x}Nb_x)_2O_7$
CURIE TEMPERATURE TC(℃)
Tc1
-107
0
(Ta)
x1
1
(Nb)
x
MIXTURE RATIO

FIG.8

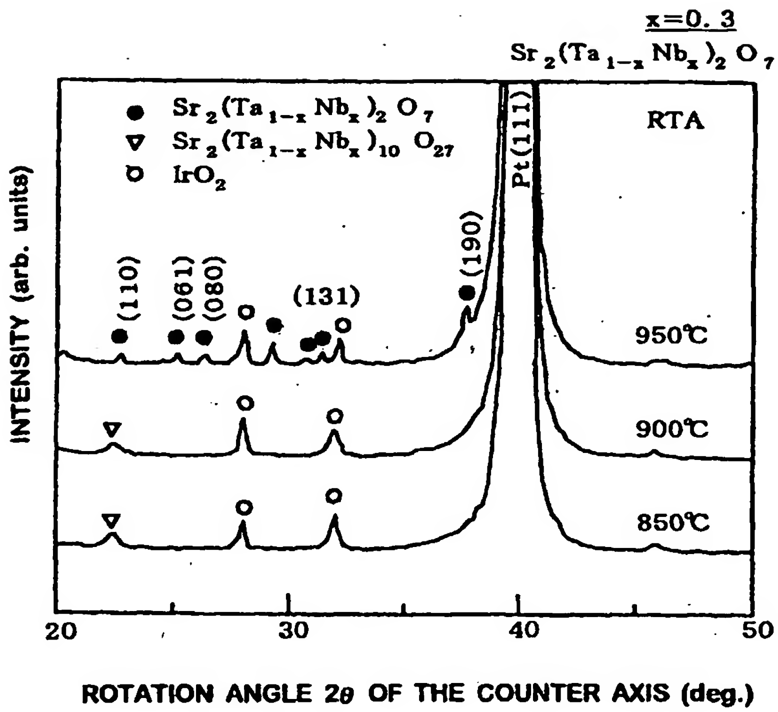
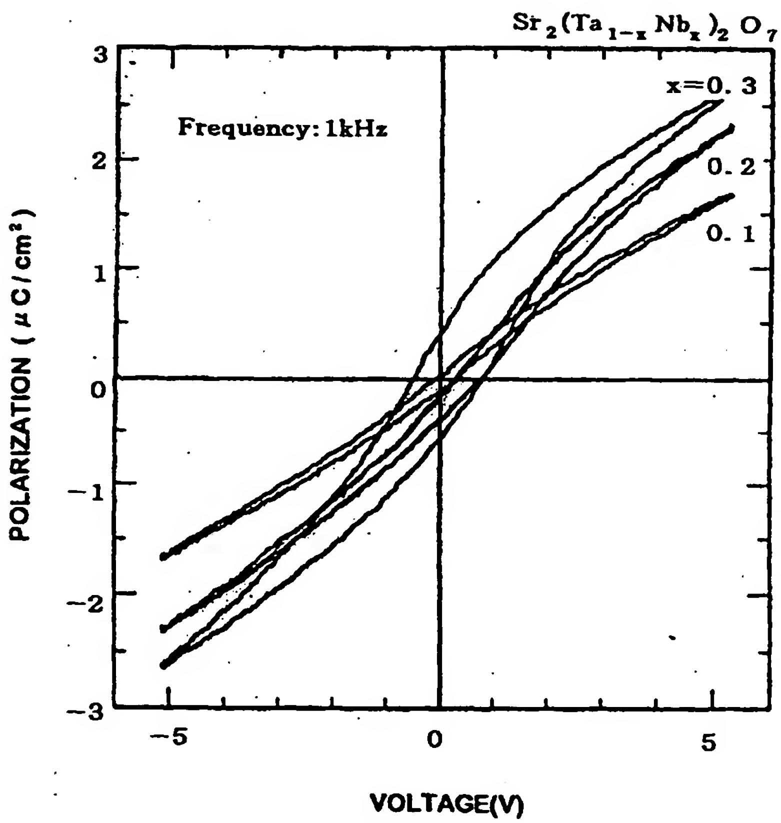

x=0. 3
$Sr_2(Ta_{1-x}Nb_x)_2O_7$
$Sr_2(Ta_{1-x}Nb_x)_2O_7$
$Sr_2(Ta_{1-x}Nb_x)_{10}O_{27}$
IrO_2
RTA
Pt(111)
(110)
(061)
(080)
(131)
(190)
950℃
900℃
850℃
INTENSITY (arb. units)
20
30
40
50
ROTATION ANGLE 2θ OF THE COUNTER AXIS (deg.)

FIG.9



$Sr_2(Ta_{1-x}Nb_x)_2O_7$
Frequency: 1kHz
x=0. 3
0. 2
0. 1
POLARIZATION ($\mu C/cm^2$)
3
2
1
0
−1
−2
−3
−5
0
5
VOLTAGE(V)

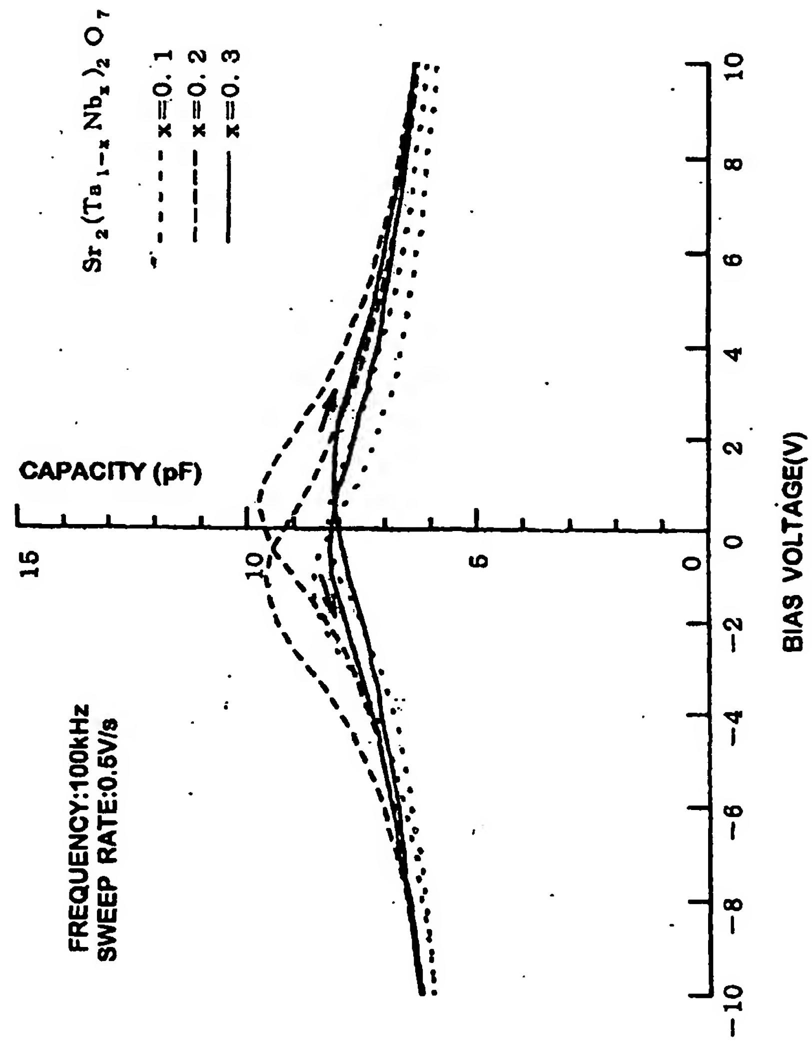

CAPACITY (pF)
15
10
5
0
BIAS VOLTAGE(V)
−10
−8
−6
−4
−2
0
2
4
6
8
10
FREQUENCY:100kHz
SWEEP RATE:0.5V/s
$Sr_2(Ta_{1-x}Nb_x)_2O_7$
x=0. 1
x=0. 2
x=0. 3

FIG.10

FIG.11

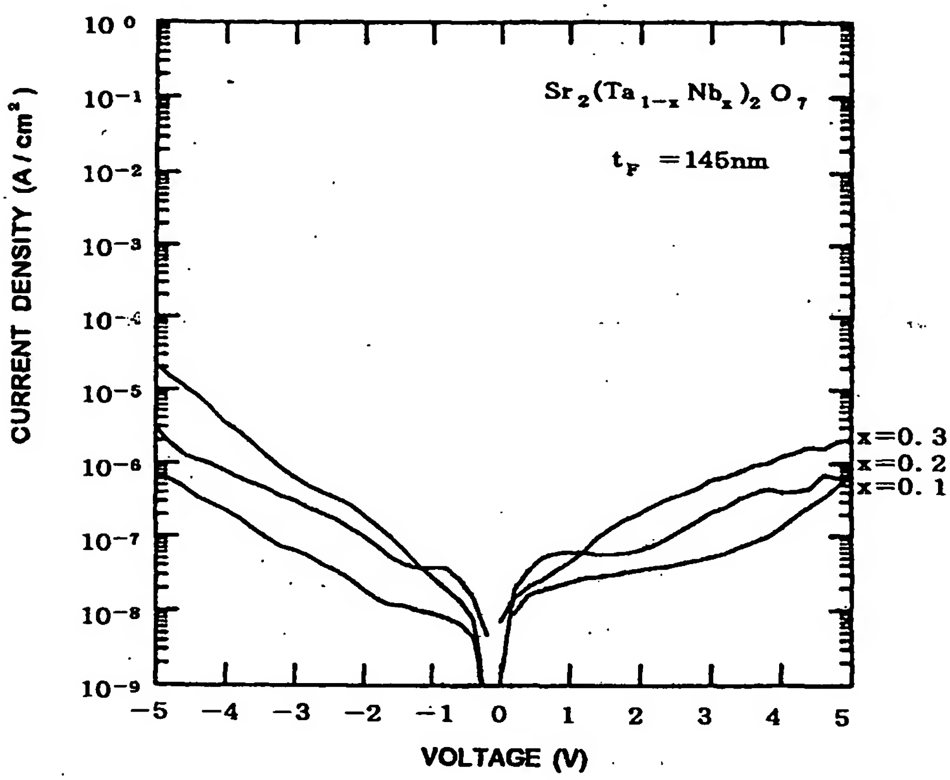

$Sr_2(Ta_{1-x}Nb_x)_2O_7$
t_F =145nm
CURRENT DENSITY (A / cm²)
VOLTAGE (V)
10⁰
10⁻¹
10⁻²
10⁻³
10⁻⁴
10⁻⁵
10⁻⁶
10⁻⁷
10⁻⁸
10⁻⁹
−5
−4
−3
−2
−1
0
1
2
3
4
5
x=0. 3
x=0. 2
x=0. 1

FIG.12A

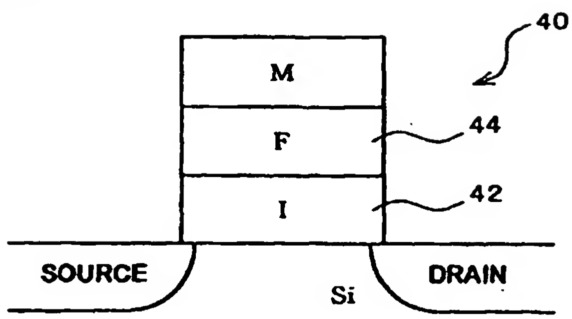


FIG.12B

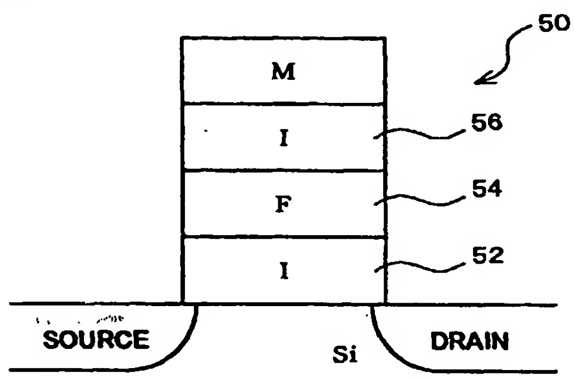


FIG.12C

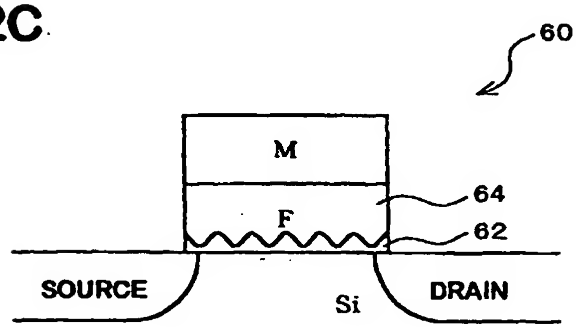
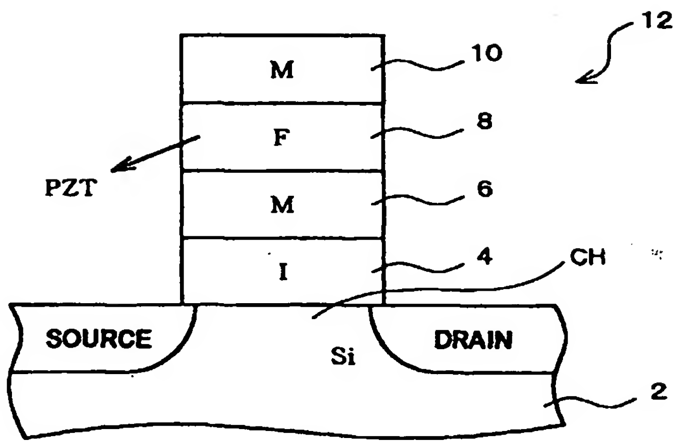


FIG.13

<PRIOR ART>



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP98/02207

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl^6 H01L29/788, 21/8247

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl^6 H01L29/788, 27/115, 21/8247

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	The 43th Preprints of the Joint Congress of Applied Physics (1996) No. 2 p.409	1-15
A	Technical Research Report of IEICE (1993) Vol. 93 No. 350 p.53-59	1-15
PX	JP, 9-213899, A (Toshiba Corp.), August 15, 1997 (15. 08. 97) (Family: none)	1-15

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
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"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
August 11, 1998 (11. 08. 98)	August 18, 1998 (18. 08. 98)

Name and mailing address of the ISA/	Authorized officer
Japanese Patent Office	
Facsimile No.	Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)